

020408 - 3
1.08

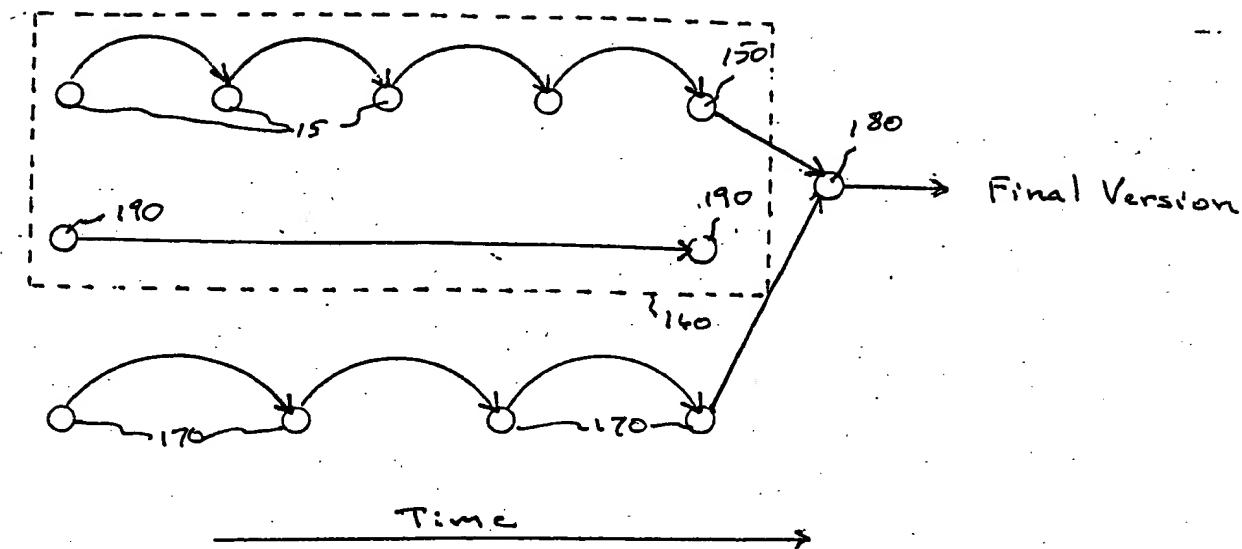


Fig. 1.

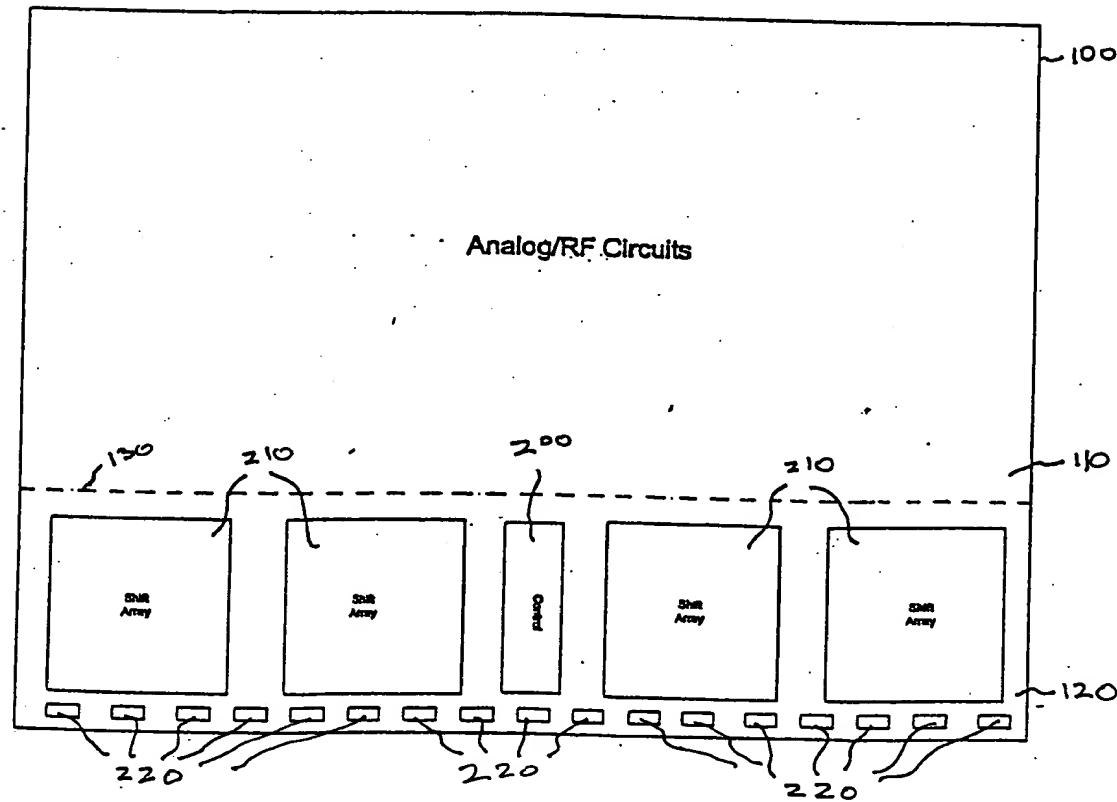


Fig. 2

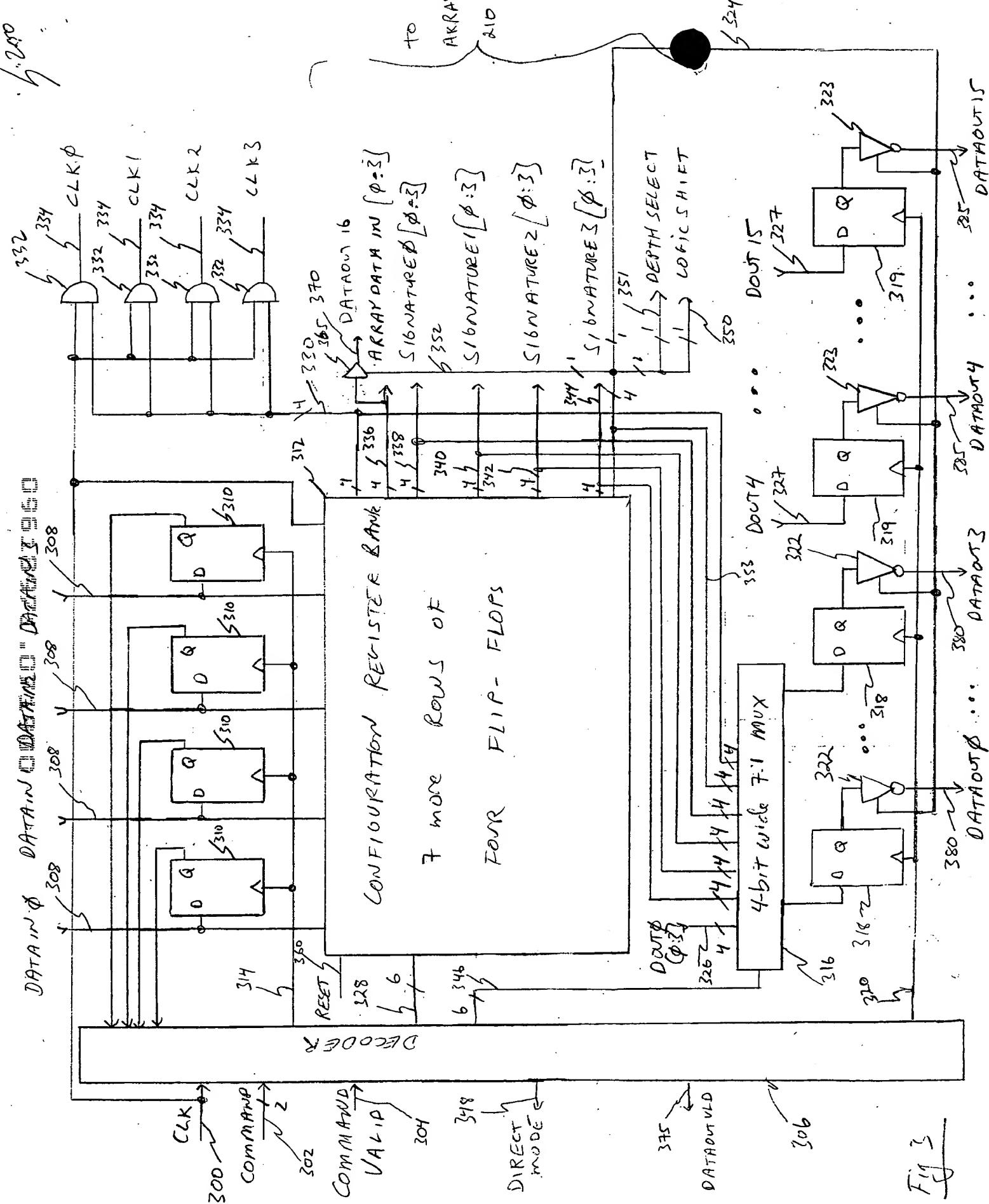
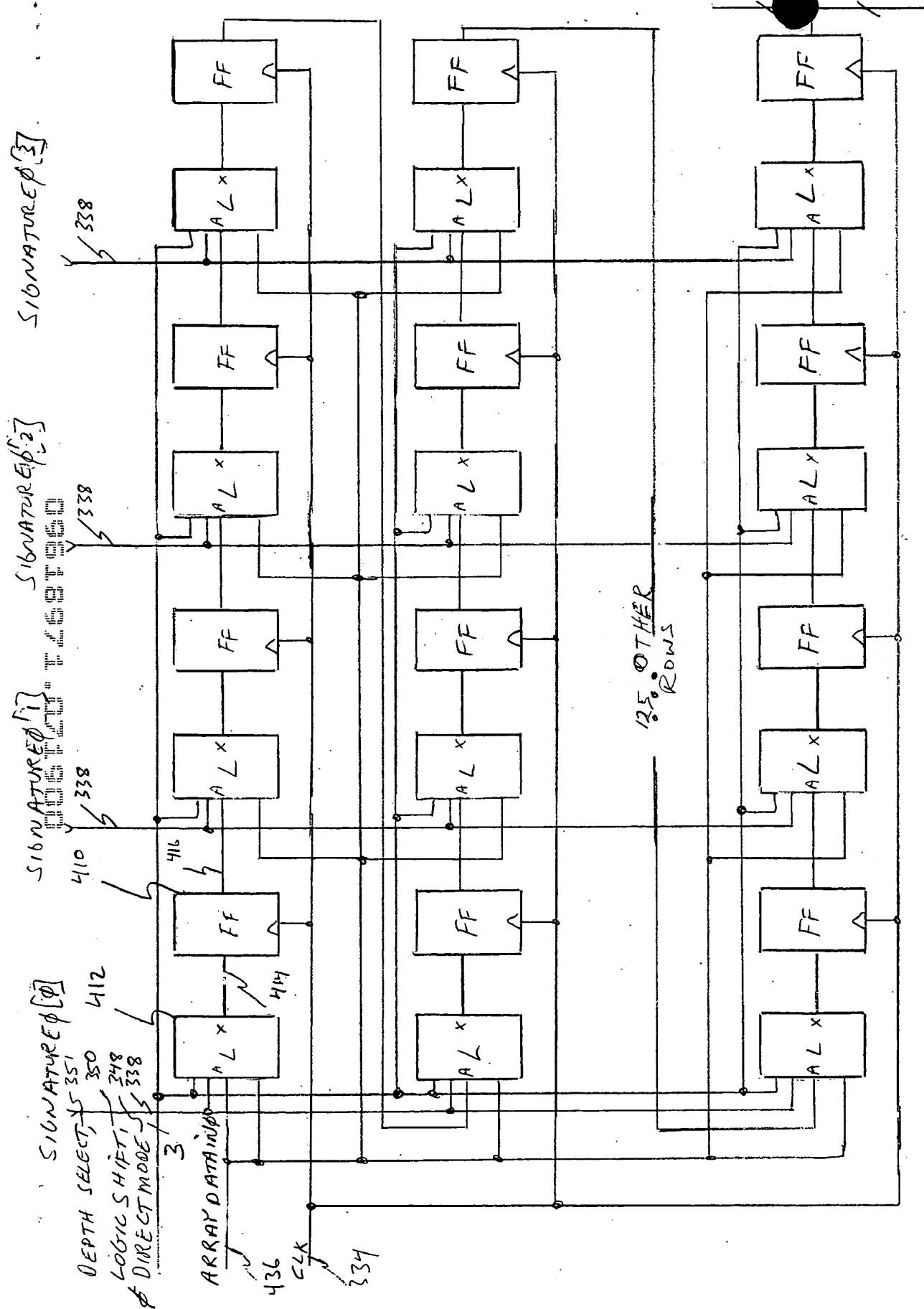


Fig 3



Array. ✓ 210

Fig. 4

Data out [3:0]

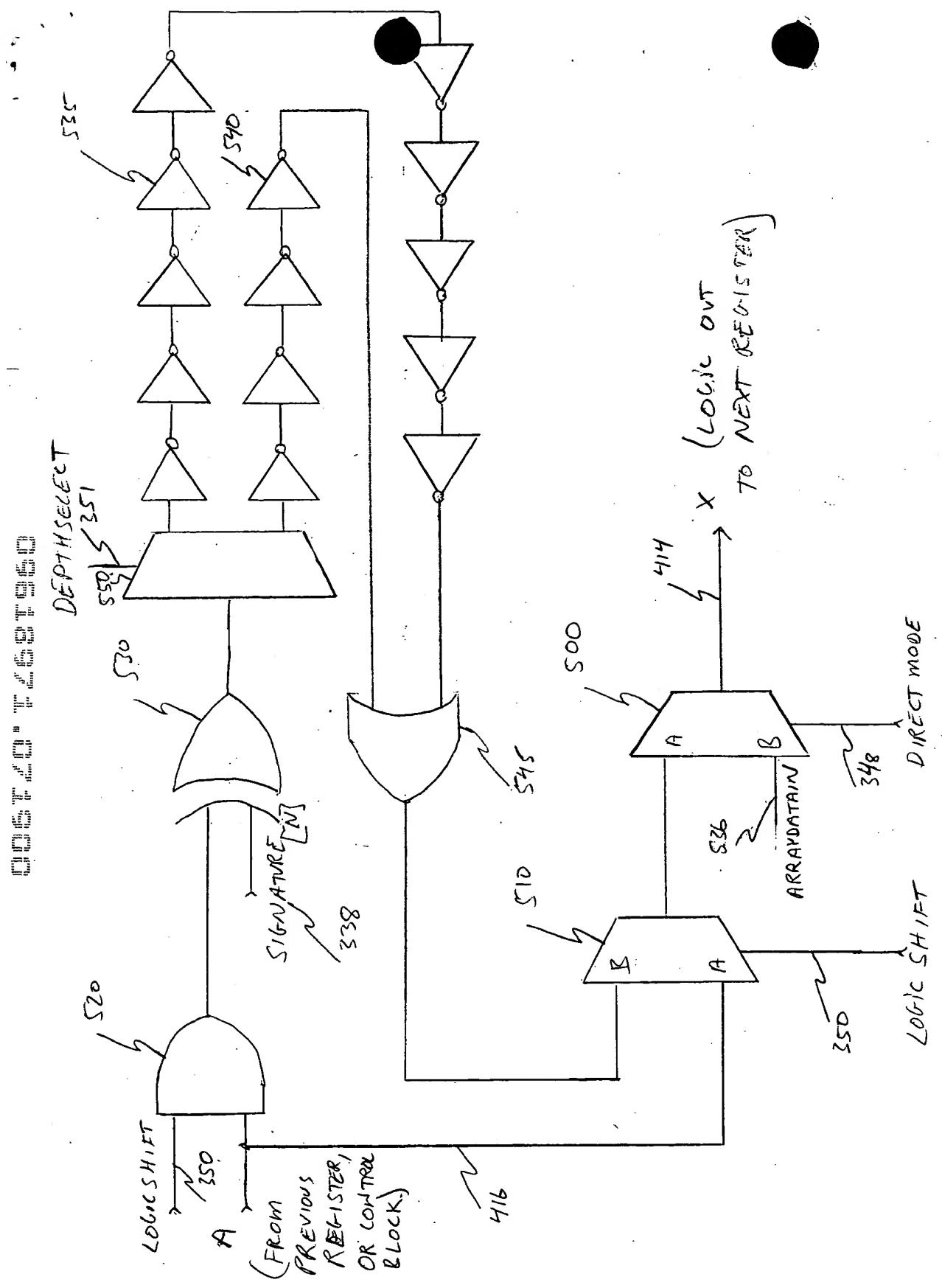


Fig. 5.

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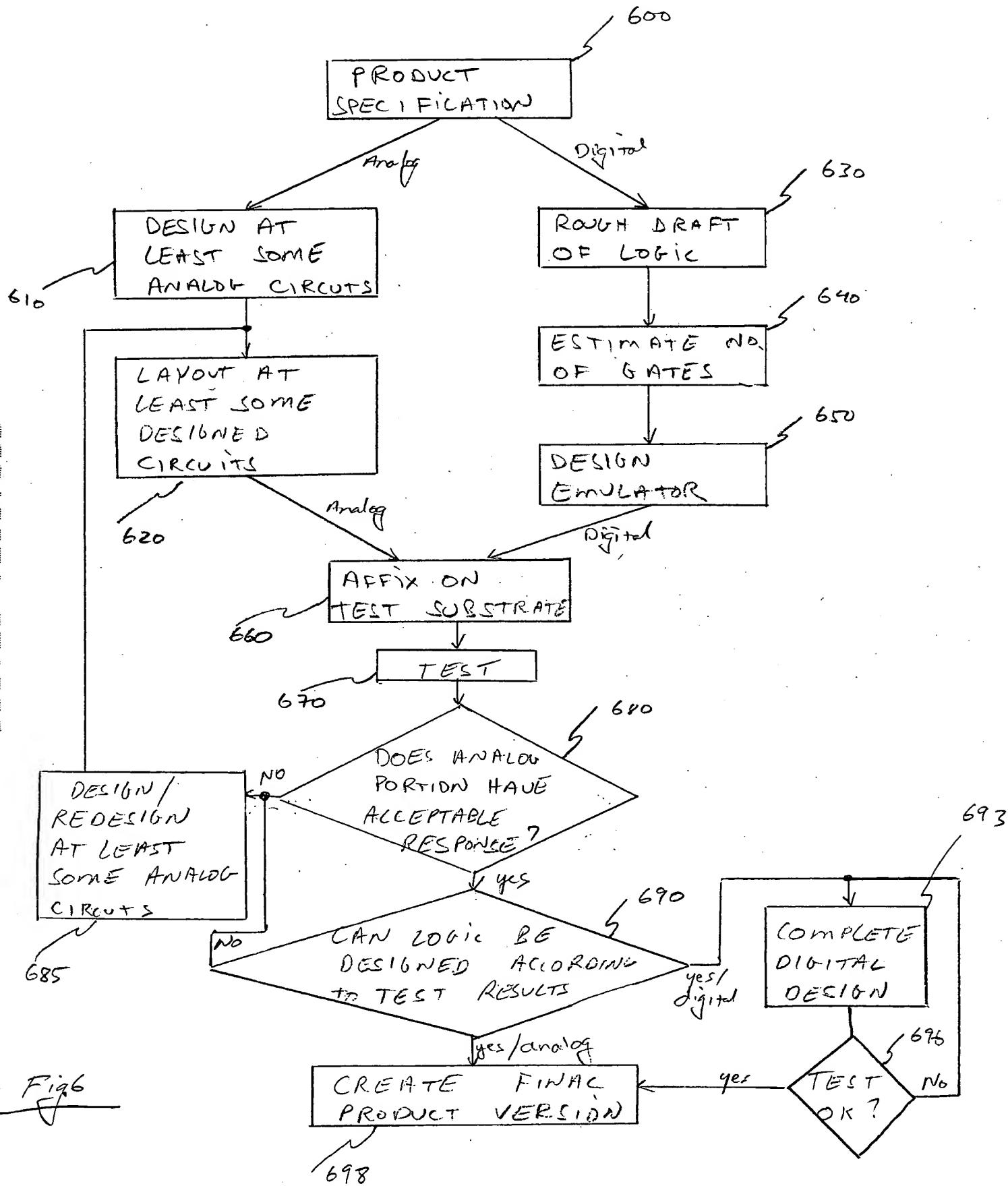


Fig 6

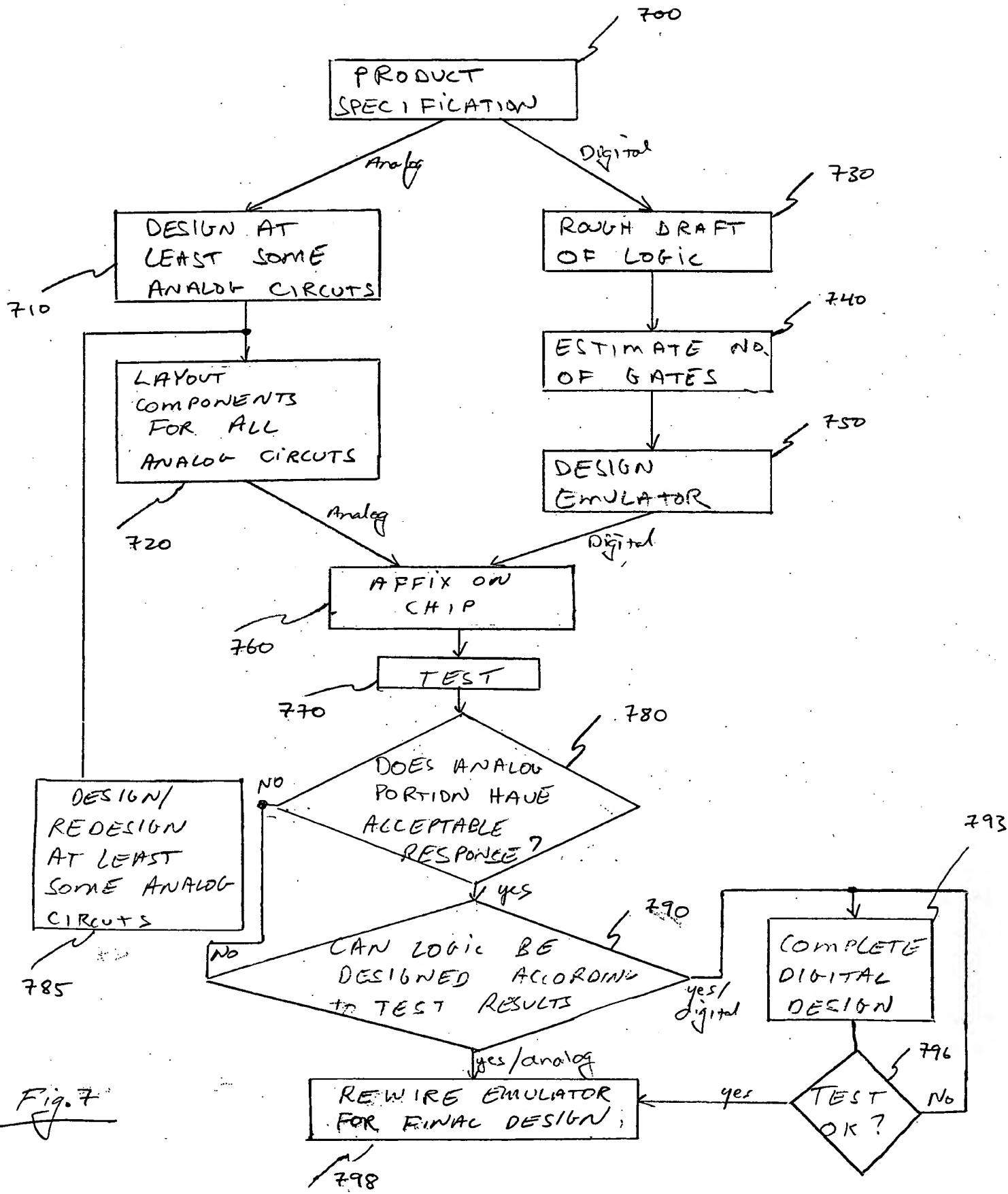
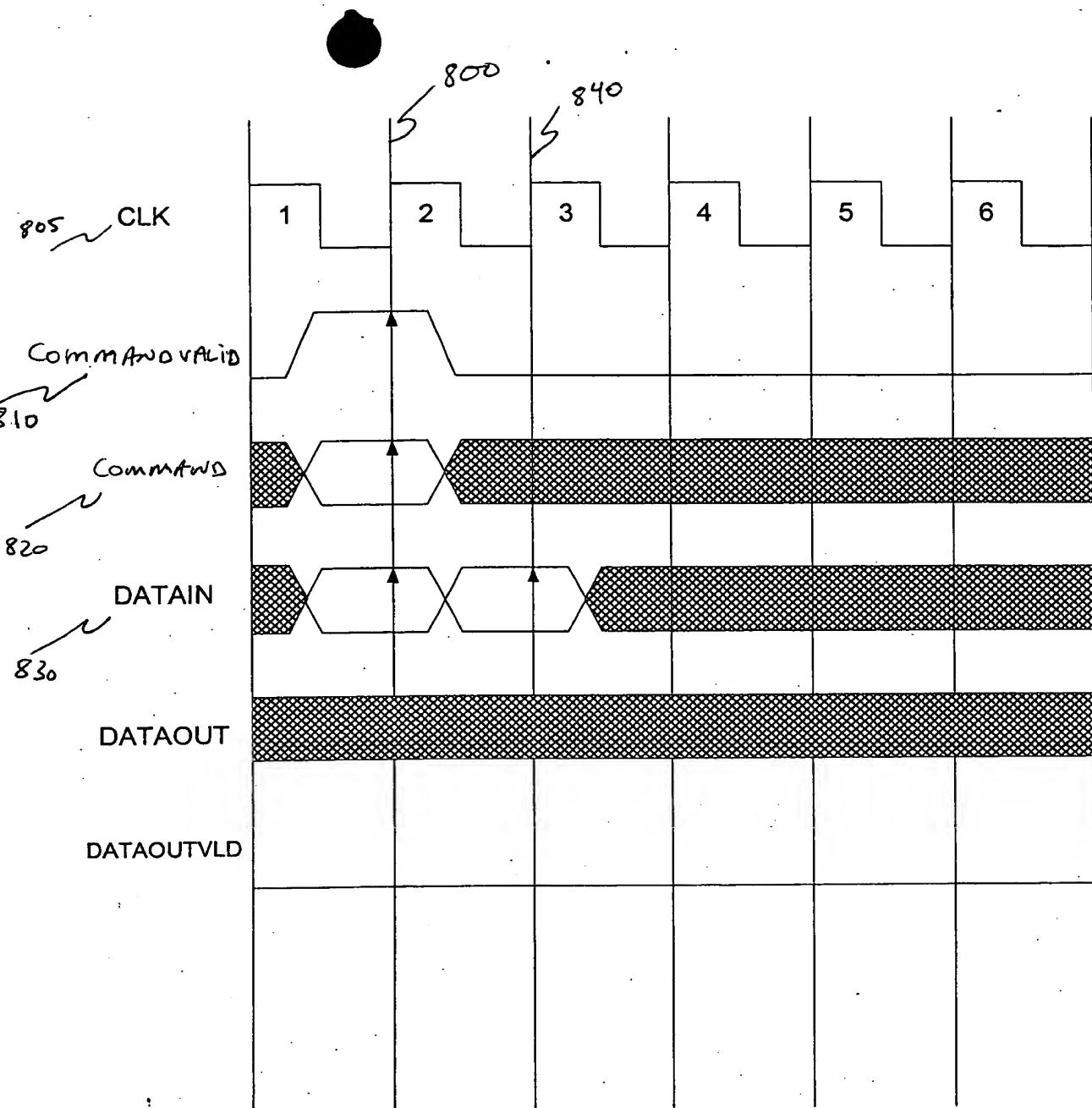
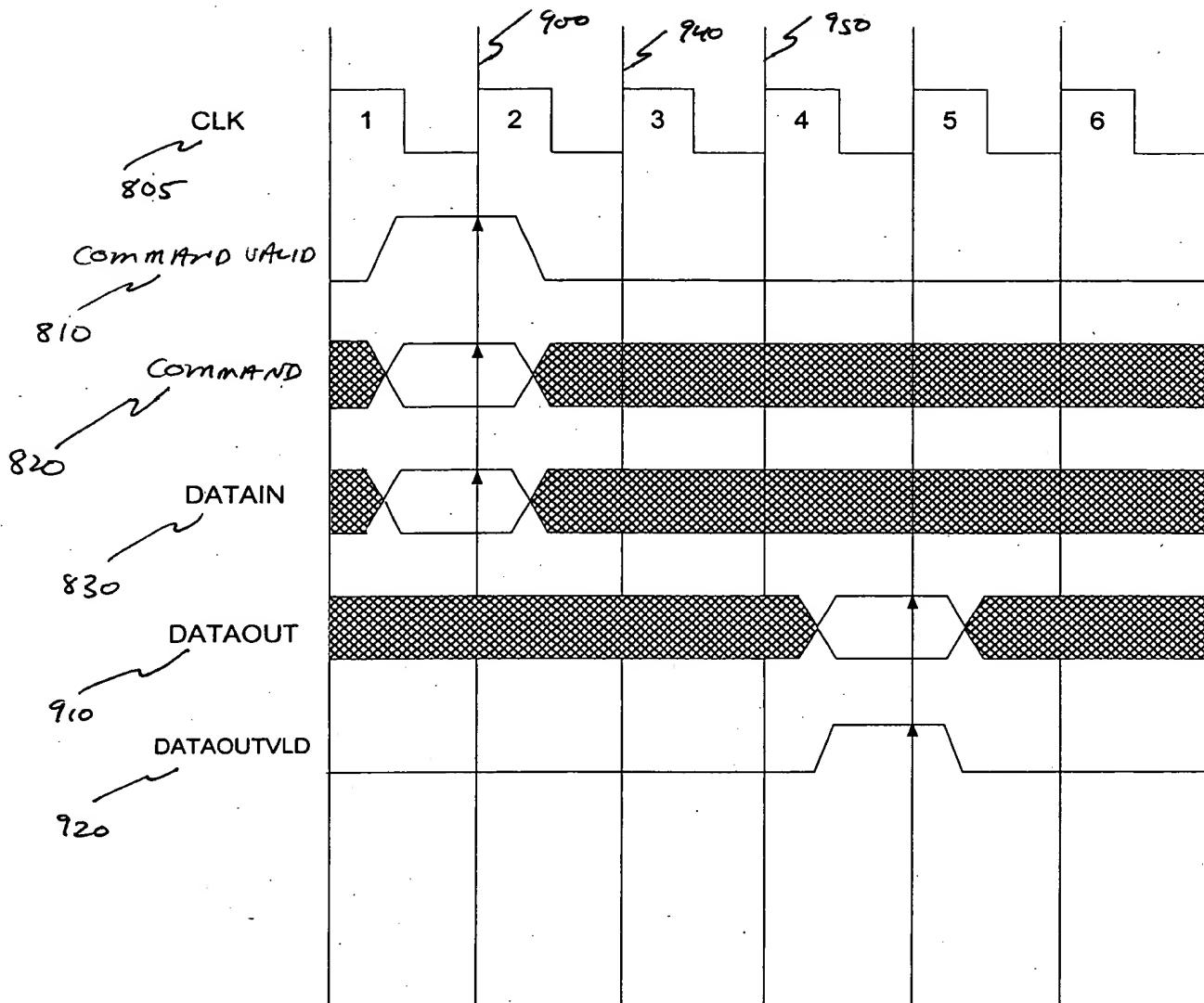


Fig. 7



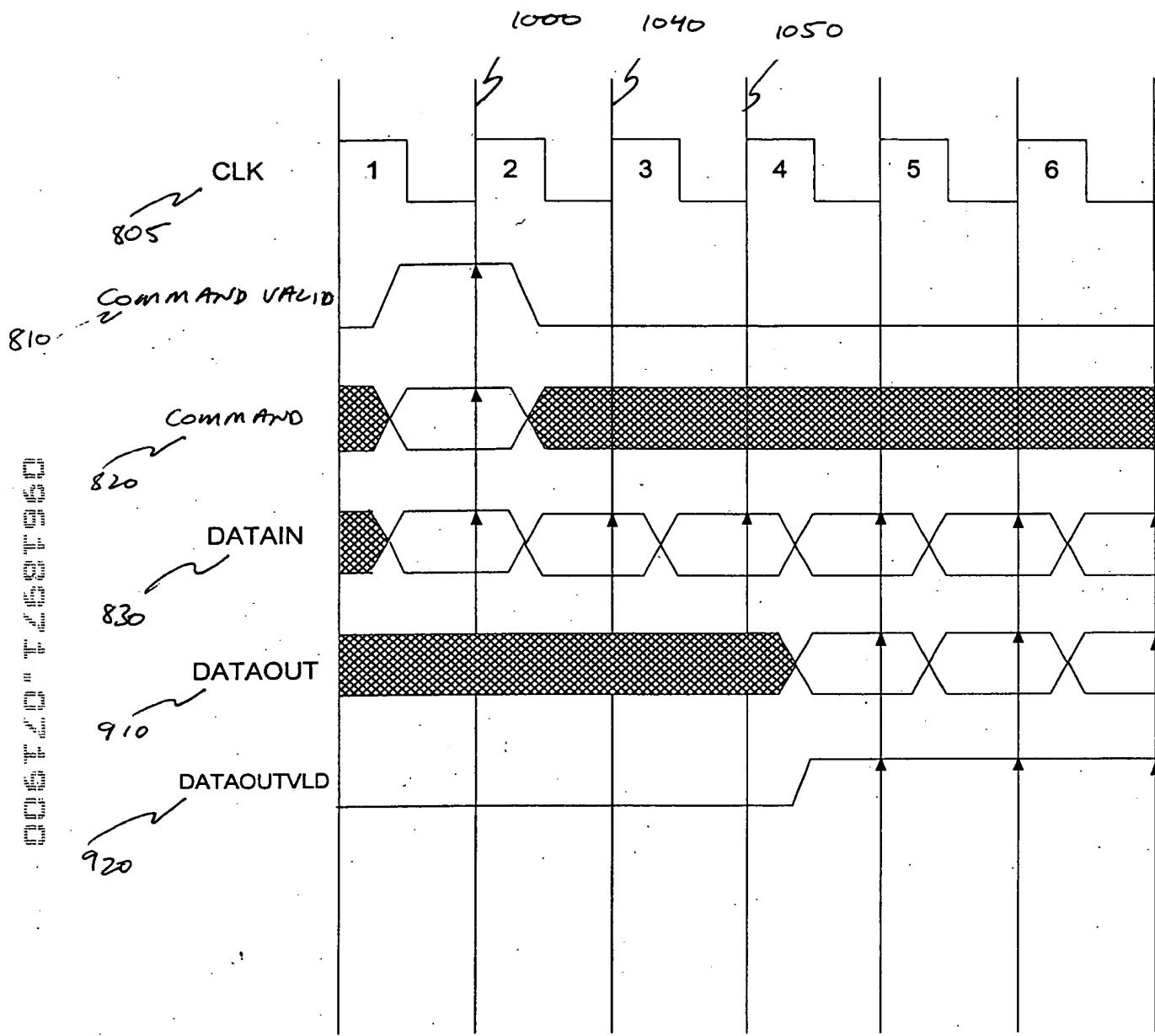
Configuration Register Write

Fig. 8



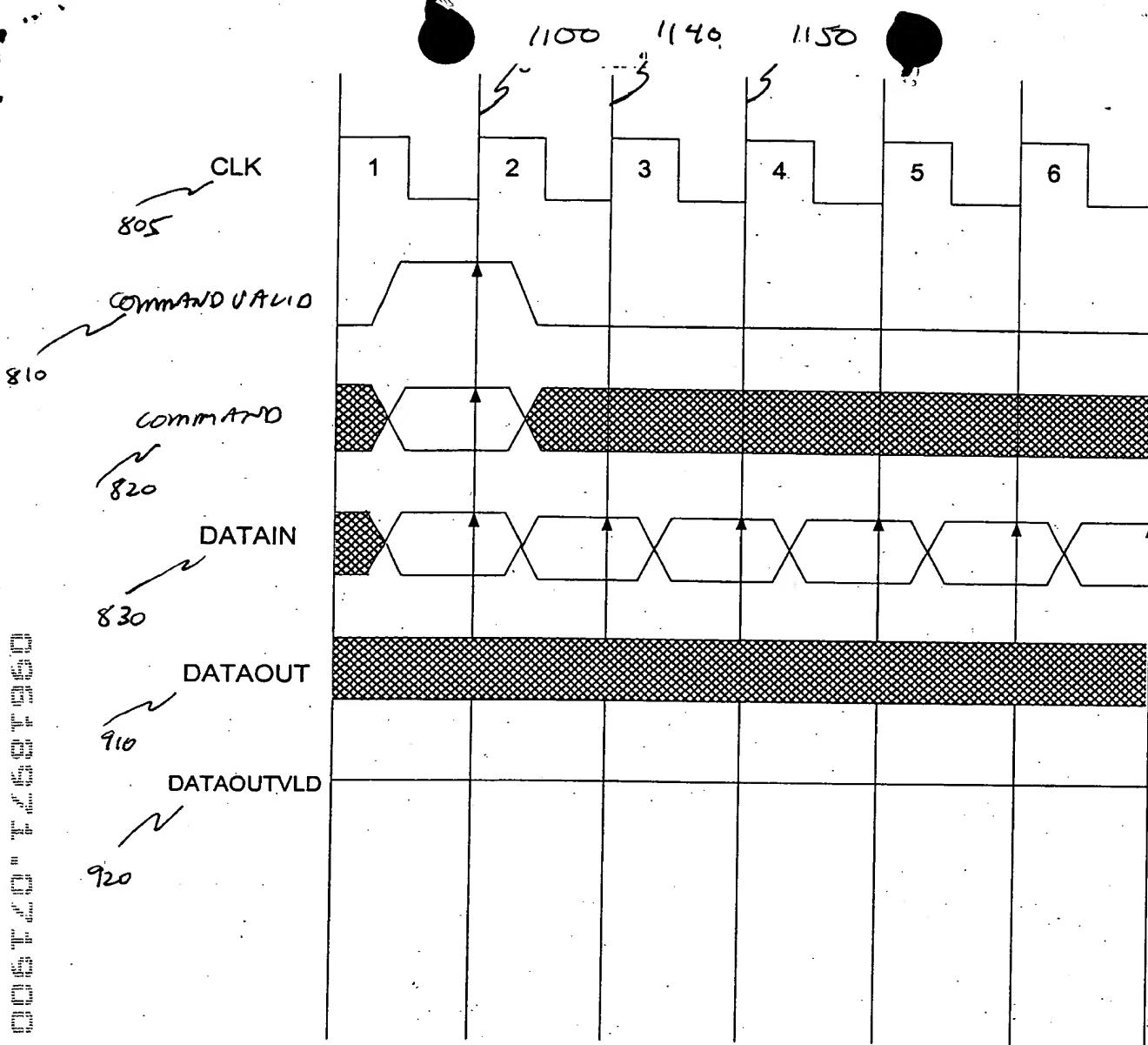
Configuration Register Read

Fig. 9



SHIFT TIMING

Fig. 10



Direct In

Fig. 11